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TITLE: ATM switch increasing switch throughput making guard time of cell buffer - delays cell output from each cell buffer at set different time by cell output delay controller, avoiding cell collision NoAbstract

PATENT-ASSIGNEE: NIPPON TELEGRAPH & TELEPHONE CORP (NITE)

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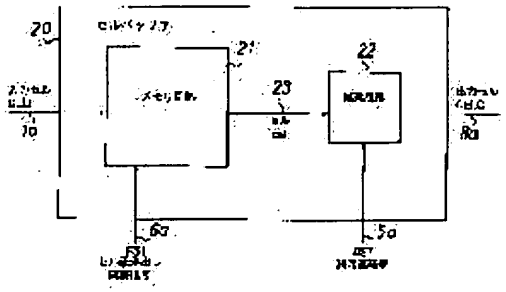
(54) ATM SWITCH

(57)Abstract:

PURPOSE: To obtain a high switch throughput characteristic by transferring a cell from each cell buffer for a cell period different from each cell buffer so as to avoid collision of cells.



CONSTITUTION: A memory circuit 21 stores cells CEL1 received via an incoming line 1a and sends cells CEL1 via a control line 23 by using a cell read synchronizing signal FST received via a control line 6a as a cell read start signal. A delay time of a delay circuit 22 is preset based on a delay value DST received via a control line 5a, and the circuit 22 gives the delay time to the signal received via the control line 23 and outputs the signal with the delay added thereto via an internal link 8a. The signal outputted from the delay circuit 22 is an output cell CELO from a cell buffer 20. Thus, the buffer circuit 20 compares the signal inputted to the circuit 21 with the signal FST and sends the output cell CELO after the delay time set via the control line 5a.

LEGAL STATUS

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* NOTICES *

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2.**** shows the word which can not be translated.
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CLAIMS

[Claim(s)]
[Claim 1] By the cel buffer which outputs the cel which it came out with two or more close circuits, the circuit was held, and it has been arranged for every above-mentioned close circuit, was inputted from this close circuit, and was accumulated temporarily to the timing of a predetermined period, and ********** arranged in the shape of a grid In the ATM switch equipped with the space switch which changes the output destination change to the above-mentioned appearance circuit of this cel based on the header information of the cel which connects between the above-mentioned close circuit and appearance circuits, and is outputted from the above-mentioned cel buffer The ATM switch characterized by only for time amount different, respectively set up beforehand delaying the output of the cel in the above-mentioned predetermined period from each above-mentioned cel buffer, and establishing the cel output delay control means which prevents a cel collision with the above-mentioned space switch.
[Claim 2] The output time delay of the cel from each above-mentioned cel buffer controlled by the above-mentioned cel output delay control means in an ATM switch according to claim 1 is an ATM switch characterized by being set up corresponding to the cel transfer time required between the cel buffer of a critical path, and a space switch.
[Claim 3] The ATM switch characterized by establishing the above-mentioned cel output delay control means in the above-mentioned cel buffer in an ATM switch given in either claim 1 or claim 2.
[Claim 4] It is the ATM switch characterized by only for time amount different, respectively set up beforehand accumulating the cel to which the above-mentioned cel output delay control means is outputted with the above-mentioned predetermined period in an ATM switch given in either of claim 1 to claims 3, and delaying the output from the above-mentioned cel buffer.
[Claim 5] It is the ATM switch characterized by only for time amount different, respectively to which the above-mentioned cel output delay control means is beforehand set in the timing of the above-mentioned predetermined period in an ATM switch given in either of claim 1 to claims 3 delaying, and delaying the output from the above-mentioned cel buffer.
[Claim 6] It is the ATM switch characterized by carrying out counting of the time amount beforehand set up with the value from which the above-mentioned cel output delay control means differs for every above-mentioned cel buffer in an ATM switch given in either of claim 1 to claims 3, determining the output initiation timing of the above-mentioned cel of each cel buffer, and delaying the output from the above-mentioned cel buffer.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to a suitable ATM switch to use for the ATM switching node which needs exchange actuation of a high-speed ATM cel especially with respect to the ATM switch used by the switching node of ATM (Asynchronous Transfer Mode: Asynchronous Transfer Mode) in broadband ISDN (service integrated digital communication network: Integrated Services Digital Network).
[0002]
[Description of the Prior Art] Some which are called ATM are in the transfer method of the information in broadband ISDN (Integrated Services DigitalNetwork, comprehensive digital communication network) like a page [177th] publication from the 168th page of "guidance of a Nikkei communication separate volume ISDN activity" (1988) of the Nikkei Business Publications issue for example. This ATM divides various information into the fixed-length block short with a header called a "cel", multiplexes and transmits it to a unit, doubles the advantage of the conventional line switching and conventional packet switching, and **** and ultra high-speed transmission are possible for it, and it can apply it also to transmission of a dynamic image.
[0003] In each ATM switching node, based on the logical channel number written in the header of the transmitted ATM cel, it comes out with the new channel number of the next destination, and a circuit (number) is decided in the communication link by such ATM. Each ATM switching node has an ATM switch, is this ATM switch, and changes and outputs the header of the transmitted ATM cel according to this label translation table.
[0004] Drawing 12 is the block diagram showing the configuration of the conventional ATM switch. In this Fig., 1a-1d are close circuits. 2a-2d an appearance circuit and 12a-12d The cel buffer arranged on close circuit 1a-1d and 3, respectively The space switch which connected ********** SWa-SWp on the grid, and 6 The synchronizing signal generating circuit and 6a which generate a cel read-out synchronizing signal The control line which connects the synchronizing signal generating circuit 6 and the cel buffers 12a-12d, 7a-7p, and 8a-8p The cel to which the internal link which connects between ********** SWa-SWp, and A-D are sent out from the cel buffers 12a-12d, and E-H are cels sent out from ********** SWm-SWp.
[0005] the cel into which the cel buffers 12a-12d are inputted from the close circuits 1a-1d, respectively -- one time -- accumulating -- control-line 6from synchronizing signal generating circuit 6 a -- minding -- all the cel buffers 12 -- the cel accumulated based on the cel read-out synchronizing signal of a fixed period (to) inputted in common is turned to a space switch 3, and is outputted to a-12d. The cel outputted from the cel buffers 12a-12d comes out in ********** [by which the appearance line number of a header unit was judged in each ********** SWa-SWp of a space switch 3, and ********** SWa-SWp has been arranged / which came out and was given to the line number and a header] SWa-SWp whose line number came out and corresponded, and is connected at Circuits 2a-2d. Thus, switching operation is performed.

[0006] However, the time amount which the cel sent out from cel buffer 12a comes out, and is outputted to 2d of circuits turns into time amount only with the long pass time D from the difference in the number of ********** to pass to [out of / E / drawing] H (3) to the time amount which the cel sent out from cel buffer 12d comes out, and is outputted to 2d of circuits. As for the time amount which similarly the cel sent out from cel buffer 12a comes out, and is outputted to 2d of circuits, only the pass time D to [out of / E / drawing] F (1) requires long time amount to the cel sent out from cel buffer 12c to the cel to which only the pass time D to [out of / E / drawing] G (2) is sent out from cel buffer 12b.
[0007] Drawing 13 is a timing diagram which shows sending-out actuation of the cel of the ATM switch in drawing 12 . Cel a is sent out from cel buffer 12a of drawing 12 , it is a period (2), Cel d is sent out from cel buffer 12d of drawing 12 , periodically (1) both shows the timing of operation at the time of aiming at 2d of appearance circuits of drawing 12 , for the inside A and D of drawing, it is an output cel from the cel buffers 12a and 12d of drawing 12 , and H is an output cel from ********** SWp of drawing 12 . By the output of ********** SWm of drawing 12 , the cel a sent out from cel buffer 12a of drawing 12 periodically (1) requires time amount alpha, and requires time amount D (3) by the output H of ********** SWp of drawing 12 from the output E of ********** SWm of drawing 12 . The cel d sent out from cel buffer 12d of drawing 12 periodically (2) requires time amount alpha by the output of ********** SWp of drawing 12 . At this time, Cel a and Cel d collide in the slash field in drawing. In order to avoid such a collision, there is a technique shown in following drawing 14 .
[0008] Drawing 14 is a timing diagram which shows the actuation for avoiding the collision of the cel in drawing 13 . After the cel a outputted from cel buffer 12a of drawing 12 used as the critical path to ********** SWp of drawing 12 is outputted from ********** SWp of drawing 12 , in order to output the cel d outputted from cel buffer 12d of drawing 12 used as the shortest path to ********** SWp of drawing 12 from ********** SWp of drawing 12 , in each cel buffer, the guard time which is the time amount which does not perform cel sending out is prepared. By this, the time delay difference produced from the difference in the number of passage ********** on an appearance circuit is compensated, and a cel collision is avoided.
[0009] However, the cel transfer period to serves as the cel sending-out time amount Tc from a cel buffer, and the sum with the maximum time delay difference D (3) at this time. Since the absolute time of the cel sending-out time amount Tc becomes short with improvement in the speed of the line speed held in an ATM switch, the time delay difference D3 becomes large seemingly. For this reason, there was a problem that took to improvement in the speed of the line speed held in an ATM switch in an ATM switch, aggravation of the utilization ratio of a circuit became remarkable, and the fall of a switch throughput became large conventionally.
[0010]
[Problem(s) to be Solved by the Invention] In a Prior art, the trouble which it is going to solve is a point that the time delay difference produced from the difference in the number of passage ********** on an appearance circuit is compensated, and the fall of the throughput of the switch accompanying improvement in the speed of a circuit cannot be avoided, in order to avoid the collision of a cel. The purpose of this invention is offering the ATM switch which solves the technical problem of these conventional technique, makes unnecessary compensation of the time delay difference produced from the difference in the number of passage ********** on an appearance circuit which was required in order to avoid the collision of a cel, outputs a cel continuously from a cel buffer, can acquire a high switch throughput property, and enables improvement in the speed of a circuit.
[0011]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the ATM switch of this invention (1) by the cel buffer which outputs the cel which it came out with two or more close circuits, the circuit was held, and it has been arranged for every close circuit, was inputted from this close circuit, and was accumulated temporarily to the timing of a predetermined period, and ********** arranged in the shape of a grid In the ATM switch equipped with the space switch which changes the output destination change to the appearance circuit of this cel based on the header information of the cel which connects between a close circuit and appearance circuits, and is outputted

from a cel buffer It is characterized by only for time amount different, respectively set up beforehand delaying the output of the cel in the predetermined period of each cel buffer, and preparing the cel output delay control section which prevents a cel collision with a space switch. Moreover, it is characterized by setting the output time delay of the cel from each cel buffer controlled by the cel output delay control section as (2) above (1) in the ATM switch of a publication corresponding to the cel transfer time required between the cel buffer of a critical path, and a space switch. Moreover, in (3) above (1) or an ATM switch given in either of (2), it is characterized by preparing a cel output delay control section in a cel buffer. Moreover, it is characterized by only for time amount different, respectively set up beforehand accumulating the cel to which a cel output delay control section is outputted with a predetermined period in an ATM switch given in either of (3) from (4) above (1), and delaying the output from a cel buffer. Moreover, only time amount different, respectively to which a cel output delay control section is beforehand set in the timing of a predetermined period in an ATM switch given in either of (5) above (1) to (3) is characterized by delaying and delaying the output from a cel buffer. Moreover, in an ATM switch given in either of (3), counting of the time amount beforehand set up with the value from which a cel output delay control section differs for every cel buffer is carried out from (6) above (1), and the output initiation timing of the cel of each cel buffer is determined, and it is characterized by delaying the output from a cel buffer.

[0012]

[Function] In this invention, in a cel transfer of a space switch, a cel transfer of each cel buffer is performed a different cel transfer period for every cel buffer, and a cel collision is avoided. This enables it to output a cel continuously from a cel buffer by there being no need of preparing the guard time which does not perform cel sending out with a cel buffer, and a high switch throughput property can be acquired.

[0013]

[Example] Hereafter, a drawing explains the example of this invention to a detail. Drawing 2 is the block diagram showing the 1st example of the configuration concerning this invention of the ATM switch of this invention. With the space switch which the ATM switch of the example of **** 1 has arranged the cel buffer for every close circuit, and has arranged ********** in the shape of a grid, it comes out with a cel buffer, and between circuits is connected, it comes out with a close circuit, and a circuit is "4."

[0014] In this Fig. a close circuit and 2a-2d 1a-1d an appearance circuit and 3 The space switch which connected ********** SWa-SWp, and 4a-4d The cel buffer (Cel B and a publication among drawing) arranged in the close circuits 1a-1d, and 5a-5d, respectively With respect to this invention, the control line into which the signal which delays an each cel buffers [4a-4d] cel output is inputted, and 6 The synchronizing signal generating circuit (the inside of drawing, SYNCK, and publication) and 6a which generate a cel read-out synchronizing signal The control line which connects the synchronizing signal generating circuit 6 and all the cel buffers 4a-4d, 7a-7p, and 8a-8p The internal link which connects between ********** SWa-SWp, and A-D are the output cels sent out from the cel buffers 4a-4d, and E-H is an output cel sent out from ********** SWm-SWp.

[0015] The cel buffers 4a-4d accumulate the cel inputted from the close circuits 1a-1d temporarily, respectively. And although the cel accumulated on the basis of the cel read-out synchronizing signal supplied common to all the cel buffers 4a-4d a period to through control-line 6a from the synchronizing signal generating circuit 6 is turned and sent out to a space switch 3 In the ATM switch of this example, it sends out after the time delay which becomes settled from the delay value beforehand set up with each cel buffers 4a-4d based on the signal inputted through the control lines 5a-5d.

[0016] Thus, in ********** SWa-SWp of a space switch 3, the cel outputted from the cel buffers 4a-4d comes out in ********** which was given to the appearance line number by which the appearance line number of a header unit is judged and ********** SWa-SWp is arranged, and a header and whose line number came out and corresponded, and is connected to a circuit.

[0017] Drawing 1 is the block diagram showing the 1st example of the configuration concerning this invention of the cel buffer in drawing 2 . The cel buffer 20 of the 1st example in this Fig. The memory

circuit 21 which accumulates the cel which shows the 1st example of a configuration of cel buffer 4a in drawing 2 , and was inputted temporarily, It is constituted with respect to this invention by the control line 23 which connects the delay circuits 22 where only predetermined time amount delays the output of a cel rather than the time amount of criteria, and these circuits, and other cel buffers 4b-4d in drawing 2 are the same configurations.

[0018] Hereafter, actuation of the cel buffer 20 is explained. A memory circuit 21 accumulates the cel CELI inputted through close circuit 1a, considers as the start signal of cel read-out of the cel read-out synchronizing signal FST inputted through control-line 6a, and sends out Cel cel through the control line 23. A delay circuit 22 outputs the signal which the time delay is set up beforehand, gave this time delay to the signal into which it is inputted through the control line 23, and gave this delay through internal link 8a based on the delay value DST inputted through control-line 5a. The signal outputted from this delay circuit 22 serves as the output cel CELO from the cel buffer 20. Thus, in the cel buffer 20 of this example, the output cel CELO is sent out as compared with the cel read-out synchronizing signal FST inputted into a memory circuit 21 to the back for the time delay set up through control-line 5a.

[0019] Drawing 3 is the block diagram showing the 2nd example of the configuration concerning this invention of the cel buffer in drawing 2 . The cel buffer 30 of the example of **** 2 shows the 2nd example of a configuration of cel buffer 4a in drawing 2 , is constituted by the control line 33 which connects the memory circuit 31 which accumulates the inputted cel temporarily, the delay circuits 32 where only predetermined time amount delays the output of a cel rather than the time amount of criteria with respect to this invention, and these circuits, and is a configuration with other same cel buffers 4b-4d in drawing 2 .

[0020] Hereafter, actuation of the cel buffer 30 is explained. A delay circuit 32 outputs cel read-out synchronizing signal FST' which the time delay is set up beforehand, gave this time delay to the cel read-out synchronizing signal FST into which it was inputted through control-line 6a, and gave this delay to a memory circuit 31 through the control line 33 based on the delay value DST inputted through control-line 5a. A memory circuit 31 accumulates the cel CELI inputted through close circuit 1a, and outputs the output cel CELO through internal link 8a as a start signal of cel read-out of cel read-out synchronizing signal FST' inputted through the control line 33.

[0021] Thus, a memory circuit 31 will send out a cel based on cel read-out synchronizing signal FST' delayed by the delay circuit 32 by the predetermined time delay, and the cel buffer 30 of this example will send out the output cel CELO after the time delay set up through control-line 5a.

[0022] Drawing 4 is a timing diagram which shows sending-out actuation of the cel concerning this invention of the ATM switch in drawing 2 . This example makes the period to which a cel is sent out from a cel buffer a cel transfer period, and sets the time amount to to. To a period (1) Cel a from cel buffer 4a of drawing 2 to a period (2) From cel buffer 4b of drawing 2 , Cel c is sent out to a period (3) from cel buffer 4c of drawing 2 , cel buffer 4d of drawing 2 to the cel d is sent out for Cel b to a period (4), and timing of operation when all cel a-d aims at 2d of appearance circuits of drawing 2 is shown. A-D shows the output cel from the cel buffers 4a-4d of drawing 2 among drawing, and E-H shows the output cel from ********** SWm-SWp of drawing 2 .

[0023] In the cel buffers 4a-4d of drawing 2 , the time delay set up from the outside through the control lines 5a-5d of drawing 2 It is based on cel buffer 4a of drawing 2 . For example, cel buffer 4b of drawing 2 The time delay D over the output cel E of the output cel F (1) and cel buffer 4c of drawing 2 cost the time delay D over the output cel E of the output cel G (2), and cel buffer 4d of drawing 2 for the time delay D over the output cel E of the output cel H (3). Thus, by setting up a time delay, it becomes possible not to depend the phase of the cel outputted from ********** SWa-SWp of drawing 2 on the cel buffer which sent out the cel, but to set it constant. A cel collision with a cel transfer period which is different when a cel is continuously sent out by this, without preparing a guard time from each cel buffer can be avoided, it becomes possible to make a cel transfer period the same as that of the cel sending-out time amount Tc from a cel buffer, and a high switch throughput property can be acquired.

[0024] Drawing 5 is the block diagram showing the 2nd example of the configuration concerning this invention of the ATM switch of this invention. With the space switch which has arranged the cel buffer

for every close circuit, and has arranged ********** in the shape of a grid like the ATM switch of the 1st example in drawing 2 , the ATM switch of the example of **** 2 comes out with a cel buffer, connects between circuits, comes out with a close circuit, and is the case where a circuit is "4."
[0025] In this Fig. a close circuit and 2a-2d 1a-1d an appearance circuit and 3 The space switch which connected ********** SWa-SWp, and 9a-9d With respect to this invention, the cel buffer arranged in the close circuits 1a-1d, and 5a-5d, respectively The control line connected to each cel buffers 9a-9d from the outside and 6 The synchronizing signal generating circuit (the inside of drawing, SYNCK, and publication) and 6a which generate a cel read-out synchronizing signal The control line which connects the synchronizing signal generating circuit 6 and all the cel buffers 9a-9d, and 10 With respect to this invention, the reference clock generating circuit (the inside of drawing, STDCK, and publication) which generates a reference clock, and 11 The control line which connects the reference clock generating circuit 10 and the cel buffers 9a-9d and 7a-7p, and 8a-8p The internal link which connects between ********** SWa-SWp, and A-D are output cels sent out from the cel buffers 4a-4d, and E-H is an output cel sent out from ********** SWm-SWp.
[0026] The cel buffers 9a-9d have the delay value which accumulates the cel inputted from the close circuits 1a-1d temporarily, respectively, and is inputted through the control lines 5a-5d. And the reference clock supplied common to all cel buffers a period Tb is inputted through the control line 11 from the reference clock generating circuit 10. Furthermore, the cel accumulated after the reference clock period corresponding to the delay value inputted into all the cel buffers 9a-9d through the control lines 5a-5d through control-line 6a from the synchronizing signal generating circuit 6 on the basis of the cel read-out synchronizing signal supplied in common the period to is sent out to a space switch 3.
[0027] Thus, in ********** SWa-SWp of a space switch 3, the appearance line number of a header unit is judged, and the cel outputted from the cel buffers 9a-9d comes out in ********** which was given to the appearance line number by which ********** SWa-SWp is arranged, and a header and whose line number comes out and corresponds, and is connected to a circuit.
[0028] Drawing 6 is the block diagram showing the 1st example of the configuration concerning this invention of the cel buffer in drawing 5 . The memory circuit 61 which accumulates the cel which the cel buffer 60 of the example of **** 1 shows the 1st example of a configuration of cel buffer 9a in drawing 5 , and was inputted temporarily, The shift register 62 which shifts the cel cel outputted through the control line 64 with respect to this invention based on the reference clock CKB inputted through the control line 11 from the memory circuit 61 one by one, and outputs it, Cels outputted with the shift register 62 are consisted of by the selector 63 which chooses and outputs the cel corresponding to the amount DST of setting delay inputted through control-line 5a, and other cel buffers 9b-9d in drawing 5 are the same configurations.
[0029] Hereafter, actuation of the cel buffer 60 is explained. A memory circuit 61 accumulates the cel CELI inputted through close circuit 1a, and sends out Cel cel to a shift register 62 through the control line 64 based on the cel read-out synchronizing signal FST of a period to inputted through control-line 6a. A shift register 62 is the circuit which connected the latch circuit of N individual to subordination, and the cel cel inputted through the control line 64 passes one latch circuit at a time for every period of the reference clock CKB of a period Tb inputted through the control line 11. Thus, a reference clock CKB can delay each cel periodic Tb every by passing one latch circuit. With a shift register 62, by passing the latch circuit of N individual, the cel Cel (N-1) which has the amount of delay of x(N-1) Tb is generated, and the outputs Ce0-Ce (N-1) of each latch circuit are outputted to a selector 63 through the control lines 65-68.
[0030] The amount of delay is beforehand set up based on the amount DST of setting delay inputted through control-line 5a, and a selector 63 minds the control lines 65-68. The cels Ce0-Ce (N-1) to which delay of N individual was given are inputted, one cel Ce with the amount of delay corresponding to the amount DST of setting delay (m) and (0 <=m<=N -1) are chosen, and the selected cel Ce (m) is outputted through internal link 4a. This cel Ce (m) turns into the output cel CELO from the cel buffer 60. This output cel CELO has the amount of delay of mxTb as compared with the cel cel outputted from the memory circuit 61, thus the cel buffer 60 of this example can control the sending-out time amount of

a cel.
[0031] Drawing 7 is a timing diagram which shows sending-out actuation of the cel concerning this invention of the cel buffer in drawing 6 . a book -- a Fig. -- setting -- FST -- a cel -- read-out -- a synchronizing signal -- it is -- Cel -- drawing 6 -- it can set -- a memory circuit -- 61 -- from -- reading -- having -- a cel -- CKB -- drawing 6 -- a shift register -- 62 -- inputting -- having -- a reference clock -- Ce -- (-- zero --) - Ce -- (-- four --) -- drawing 6 -- it can set -- a shift register -- 62 -- from -- an output -- a cel -- CELO -- drawing 6 -- it can set -- a cel -- a buffer -- 60 -- from -- an output -- a cel -- it is -- the bit of the shadow area of each cel -- a cel head bit -- it is . It is the case where this example set the amount (DST) of setting delay to Tb which is one period of a reference clock CKB, and a time delay generable [with the shift register 62 of drawing 6] is set to 0, 1 and Tb, 2 and Tb, 3 and Tb, and 4 and Tb, and Cel Ce (1) is chosen by the selector 63 of drawing 6 as an output cel CELO from the shift register 62 of drawing 6 on such conditions. Thus, only Tb time amount equivalent to one period of a reference clock CKB can delay the output of the cel CELO from the cel buffer 60 in drawing 6 .
[0032] Drawing 8 is the block diagram showing the 2nd example of the configuration concerning this invention of the cel buffer in drawing 5 . The memory circuit 81 which accumulates the cel which the cel buffer 80 of the example of **** 2 shows the 2nd example of a configuration of cel buffer 9a in drawing 5 , and was inputted temporarily, The shift register 82 which shifts the cel read-out synchronizing signal FST inputted through control-line 6a with respect to this invention based on the reference clock CKB inputted through the control line 11 one by one, and outputs it, It is constituted by the selector 83 which chooses and outputs the thing corresponding to the amount DST of setting delay inputted through control-line 5a among the cel read-out synchronizing signals FST from a shift register 82, and other cel buffers 9b-9d in drawing 5 are the same configurations.
[0033] Hereafter, actuation of the cel buffer 80 is explained. A shift register 82 is the circuit which connected the latch circuit of N individual to subordination, and the cel read-out control signal FST of a period To inputted through control-line 6a passes one latch circuit at a time for every period of the reference clock CKB of a period Tb inputted through the control line 11. Thus, a reference clock CKB can delay the cel read-out synchronizing signal FST periodic Tb every by passing one latch circuit. And by passing the latch circuit of N individual, the cel read-out synchronizing signal Fr (N-1) which has the amount of delay of x(N-1) Tb is generated, and output Fr(0) -Fr (N-1) of each latch circuit is outputted to a selector 83 through the control lines 85-88.
[0034] The amount of delay is beforehand set up based on the amount DST of setting delay as which a selector 83 is inputted through control-line 5a. From cel read-out synchronizing signal Fr(0) -Fr (N-1) of N individual inputted through the control lines 85-88 to which delay was given, respectively One cel read-out synchronizing signal Fr with the amount of delay corresponding to the amount DST of setting delay (m) and (0 <=m<=N -1) are chosen, and this selected cel read-out synchronizing signal Fr (m) is outputted to a memory circuit 81 through the control line 84. A memory circuit 81 accumulates the cel CELI inputted from input circuit 1a, is chosen by the selector 83, and sends out the output cel CELO for the cel read-out synchronizing signal Fr (m) inputted through the control line 84 through internal link 4a as a signal of cel read-out initiation.
[0035] Thus, as compared with the cel read-out synchronizing signal FST inputted into a shift register 82, the cel read-out synchronizing signal Fr (m) outputted from a selector 83 has the amount of delay of mxTb, and can control the cel sending-out time amount from the buffer of a cel by making this cel read-out synchronizing signal Fr (m) into the start signal of cel read-out.
[0036] Drawing 9 is a timing diagram which shows sending-out actuation of the cel concerning this invention of the cel buffer in drawing 8 . In this Fig., FST and CKB are the cel read-out synchronizing signals and reference clocks which are inputted into the shift register 82 of drawing 8 , it is an output from the cel buffer [in / Fr(0) -Fr(4) from the shift register 82 of drawing 8 to an output, and / in CELO / drawing 8] 60, and the bit of the shadow area of each cel is a cel head bit. This example is the case where set the amount of setting delay (4ST) to Tb which is one period of a reference clock CKB, and the amount of delay generated with the shift register 82 of drawing 8 is set to 0, 1 and Tb, 2 and Tb, 3 and Tb, and 4 and Tb. On such conditions, Fr (1) is chosen from the output of the shift register 82 of

drawing 8 by the selector 83 of drawing 8 , and Cel CELO is outputted from the memory circuit 81 of drawing 8 based on this Fr (1). Thus, only Tb time amount equivalent to one period of a reference clock CKB can delay the cel output from the cel buffer 80 in drawing 8.

[0037] Drawing 10 is the block diagram showing the 3rd example of the configuration concerning this invention of the cel buffer in drawing 5 . The memory circuit 101 which accumulates the cel which the cel buffer 100 of the example of **** 3 shows the 3rd example of a configuration of cel buffer 9a in drawing 5 , and was inputted temporarily, The counter 102 which counts the reference clock CKB inputted through the control line 11 with respect to this invention based on the count effective synchronizing signal FCT inputted through control-line 6a (counting), It is constituted by the comparator circuit 103 which compares the counted value from a counter 102 based on the amount DST of setting delay into which it is inputted through control-line 5a, and other cel buffers 9b-9d in drawing 5 are the same configurations.

[0038] Hereafter, actuation of the cel buffer 100 is explained. A counter 102 inputs the count effective synchronizing signal FCT for a reference clock CKB through control-line 6a again through the control line 11, from the standup of the count effective synchronizing signal FCT, starts the count of the number of inputs of a reference clock CKB, and outputs the counted value NUM to a comparator circuit 103 through the control line 104. In addition, a counter 102 resets counted value, when counted value reaches the maximum which a counter 102 has.

[0039] A comparator circuit 103 inputs the amount DST of setting delay for the counted value NUM from a counter 102 through control-line 5a again through the control line 104, and compares both values. This amount DST of setting delay shows the time amount Do which sends out a cel from a memory circuit 101, and is beforehand set up in a comparator circuit 103. And when counted value NUM is in agreement with the time amount Do which becomes settled in the amount DST of setting delay, the cel read-out synchronizing signal FST is outputted to a memory circuit 101 through the control line 105. A memory circuit 101 accumulates the cel CELI inputted through close circuit 1a, and sends out the output cel CELO through internal link 4a as a start signal of cel read-out of the cel read-out signal FST inputted through the control line 105.

[0040] Since only time amount Do is delayed and is outputted as compared with the count effective synchronizing signal FCT inputted into a counter 102, when the cel read-out synchronizing signal FST outputted from the comparator circuit circuit 103 reads Cel CELO from a memory circuit 101 based on the cel read-out synchronizing signal FST, the cel sending-out time amount from the cel buffer 100 can be delayed.

[0041] Drawing 11 is a timing diagram which shows sending-out actuation of the cel concerning this invention of the cel buffer in drawing 10 . In this Fig., FCT and CKB are the count effective synchronizing signal inputted into the counter 102 of drawing 10 , and a reference clock, respectively. NPO1 and NPO1 The counter value expressed with 2 bits outputted from the counter 102 of drawing 10 , and DST0 and DST1 The amount of setting delay and FST which were expressed with 2 bits inputted into the comparator circuit 103 of drawing 10 The cel read-out synchronizing signal sent out to a memory circuit 101 from the comparator circuit 103 in drawing 10 and CELO are the outputs from the cel buffer 100 in drawing 10 , and the bit of the shadow area of each cel is a cel head bit.

[0042] This example is the case where set the amount (DST) of setting delay to Tb which is one period of a reference clock CKB, and it considers as the case where the maximum of the counter 102 of drawing 10 is "4." On such conditions, after the count effective synchronizing signal FCT is inputted into the counter 102 of drawing 10 and a reference clock CKB is inputted once into it, the value of the counter 102 of drawing 10 is set to "1", and serves as a set-up time delay. At this time, from the comparator circuit 103 of drawing 10 , the cel read-out synchronizing signal FST is generated, it is outputted to the memory circuit 101 of drawing 10 , and Cel CELO is outputted based on this cel read-out synchronizing signal FST by the memory circuit 101 of drawing 10 . By the above actuation, only Tb time amount equivalent to one period of a reference clock CKB can delay the output of the cel from the cel buffer 100 of drawing 10 .

[0043] As mentioned above, as explained using drawing 1 - drawing 11 , with the ATM switch of this

example, in a cel transfer of a space switch, each cel buffer performs a transfer of a cel a different cel transfer period for every cel buffer, and avoids a cel collision. By this, with a cel buffer, there is no need of preparing the guard time which does not perform cel sending out, and the fall of the throughput of the switch accompanying improvement in the speed of a circuit can be avoided (since the time delay difference produced from the difference in the number of passage ********** on an appearance circuit is compensated). In addition, this invention is not limited to the example explained using drawing 1 - drawing 11 , and can be variously changed in the range which does not deviate from the summary.
[0044]
[Effect of the Invention] According to this invention, compensation of the time delay difference produced from the difference in the number of passage ********** on an appearance circuit which was required in order to avoid the collision of a cel conventionally becomes unnecessary, a cel is continuously outputted from a cel buffer, a high switch throughput property can be acquired, and improvement in the speed of a circuit is possible.
[0045]

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the 1st example of the configuration of the cel buffer concerning this invention.
[Drawing 2] It is the block diagram showing the 1st example of the configuration concerning this invention of the ATM switch of this invention.
[Drawing 3] It is the block diagram showing the 2nd example of the configuration concerning this invention of the cel buffer in drawing 2 .
[Drawing 4] It is the timing diagram which shows sending-out actuation of the cel concerning this invention of the ATM switch in drawing 2 .
[Drawing 5] Drawing 5 is the block diagram showing the 2nd example of the configuration concerning this invention of the ATM switch of this invention.
[Drawing 6] It is the block diagram showing the 1st example of the configuration concerning this invention of the cel buffer in drawing 5 .
[Drawing 7] It is the timing diagram which shows sending-out actuation of the cel concerning this invention of the cel buffer in drawing 6 .
[Drawing 8] It is the block diagram showing the 2nd example of the configuration concerning this invention of the cel buffer in drawing 5 .
[Drawing 9] It is the timing diagram which shows sending-out actuation of the cel concerning this invention of the cel buffer in drawing 8 .
[Drawing 10] It is the block diagram showing the 3rd example of the configuration concerning this invention of the cel buffer in drawing 5 .
[Drawing 11] It is the timing diagram which shows sending-out actuation of the cel concerning this invention of the cel buffer in drawing 10 .
[Drawing 12] It is the block diagram showing the configuration of the conventional ATM switch.
[Drawing 13] It is the timing diagram which shows the example of sending-out actuation of the cel of the ATM switch in drawing 12 .
[Drawing 14] It is the timing diagram which shows the example of operation for avoiding the collision of the cel in drawing 13 .
[Description of Notations]
1a-1d Close circuit
2a-2d Appearance circuit
3 Space Switch
4a-4d Cel buffer
5a-5d Control line
6 Synchronizing Signal Generating Circuit
6a Control line
7a-7p Internal link
8a-8p Internal link

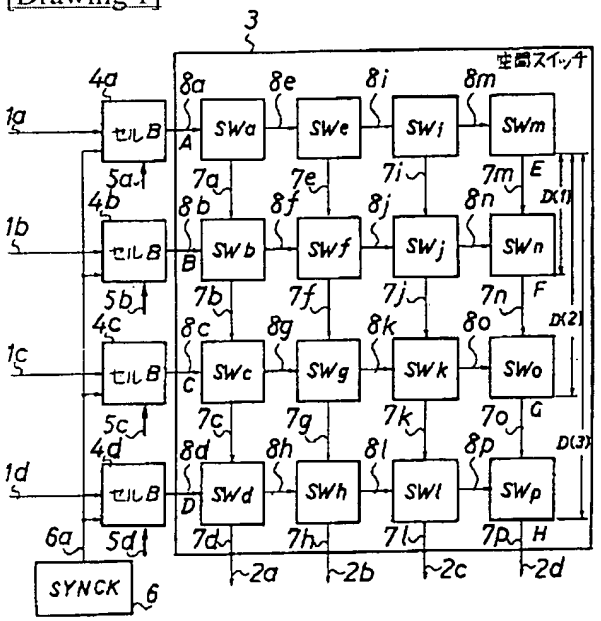
9a-9d Cel buffer
10 Reference Clock Generating Circuit
11 Control Line
12a-12d Cel buffer
20 Cel Buffer
21 Memory Circuit
22 Delay Circuit
23 Control Line
30 Cel Buffer
31 Memory Circuit
32 Delay Circuit
33 Control Line
60 Cel Buffer
61 Memory Circuit
62 Shift Register
63 Selector
64-68 Control line
80 Cel Buffer
81 Memory Circuit
82 Shift Register
83 Selector
84-88 Control line
100 Cel Buffer
101 Memory Circuit
102 Shift Register
103 Selector
104 105 Control line
A-H Cel
SWa-SWp **********

[Translation done.]

* NOTICES *

DRAWINGS

[Drawing 1]



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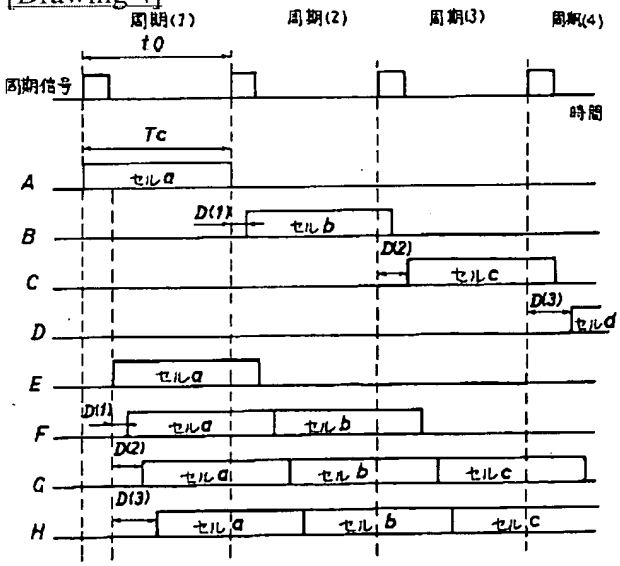
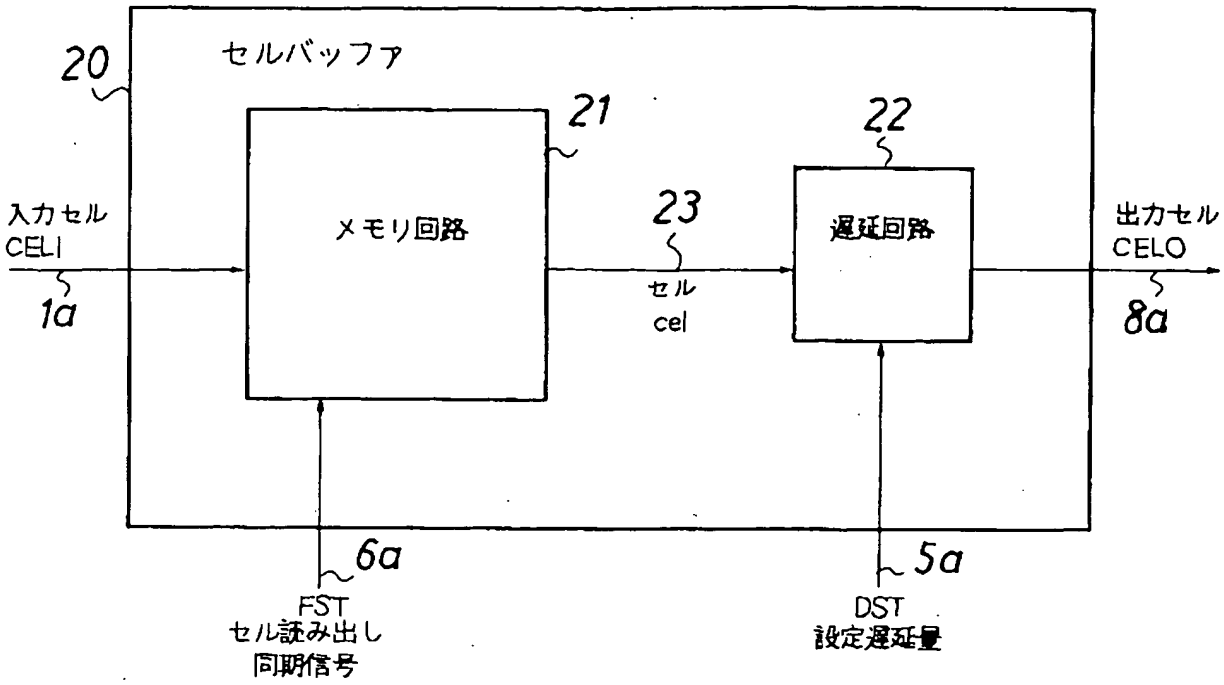
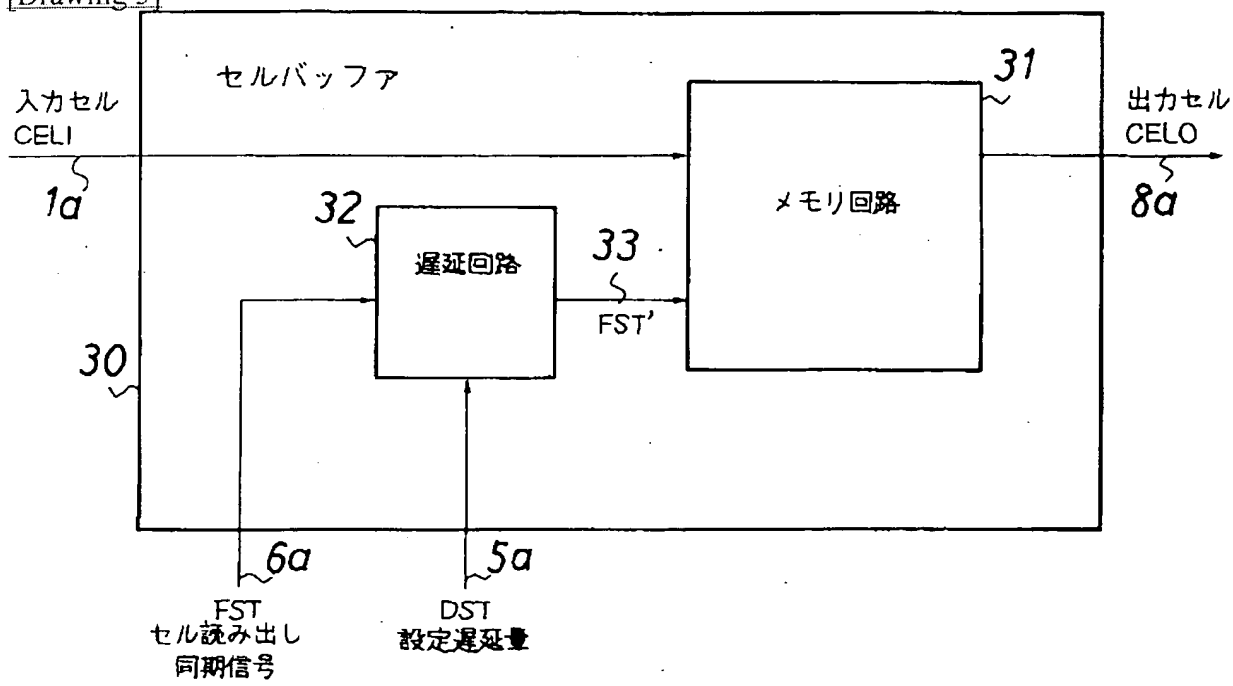


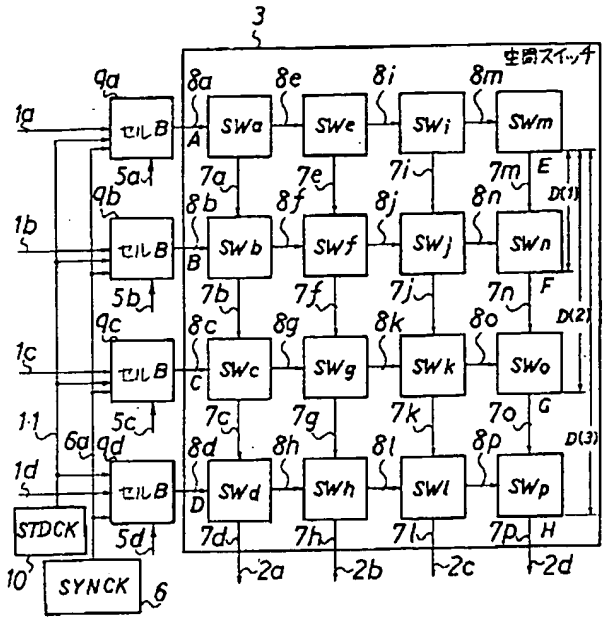
[Drawing 2]



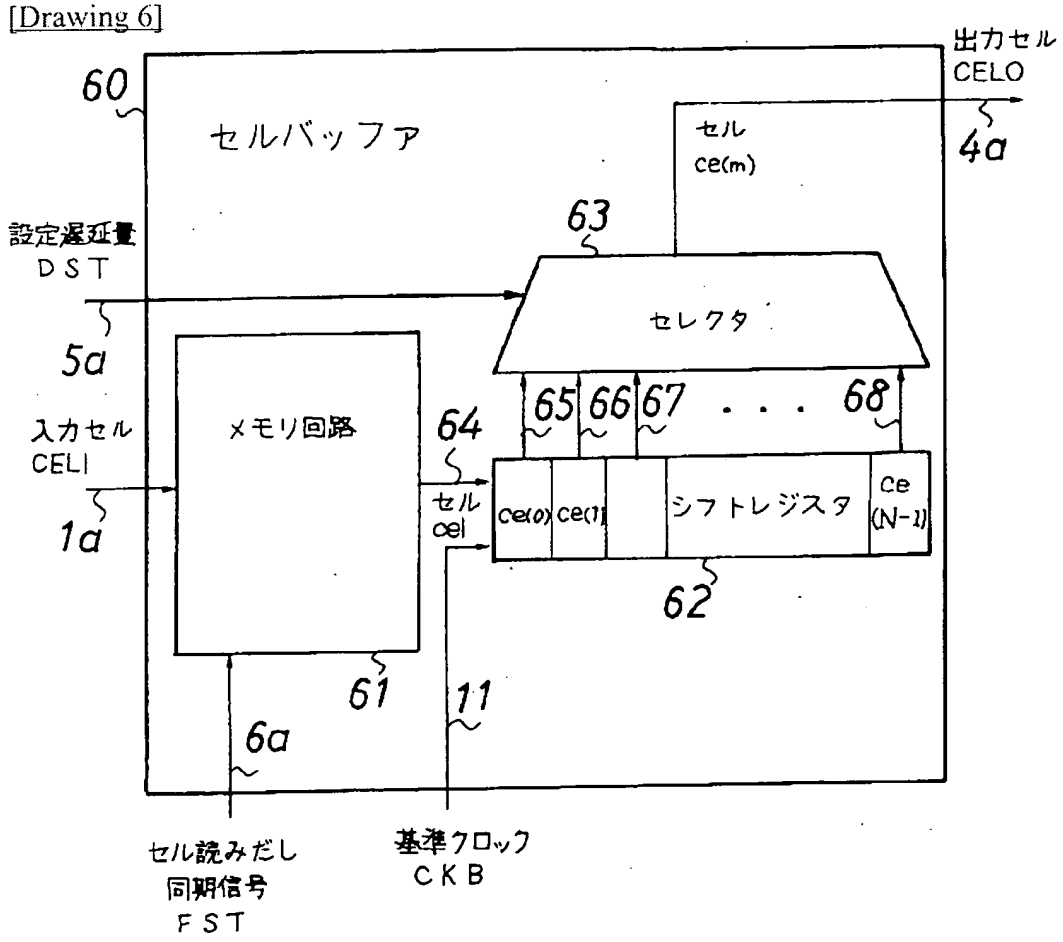
[Drawing 3]



[Drawing 5]



[Drawing 6]



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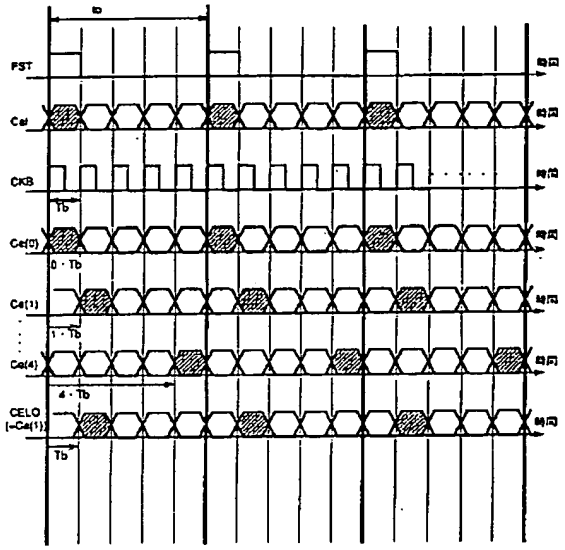

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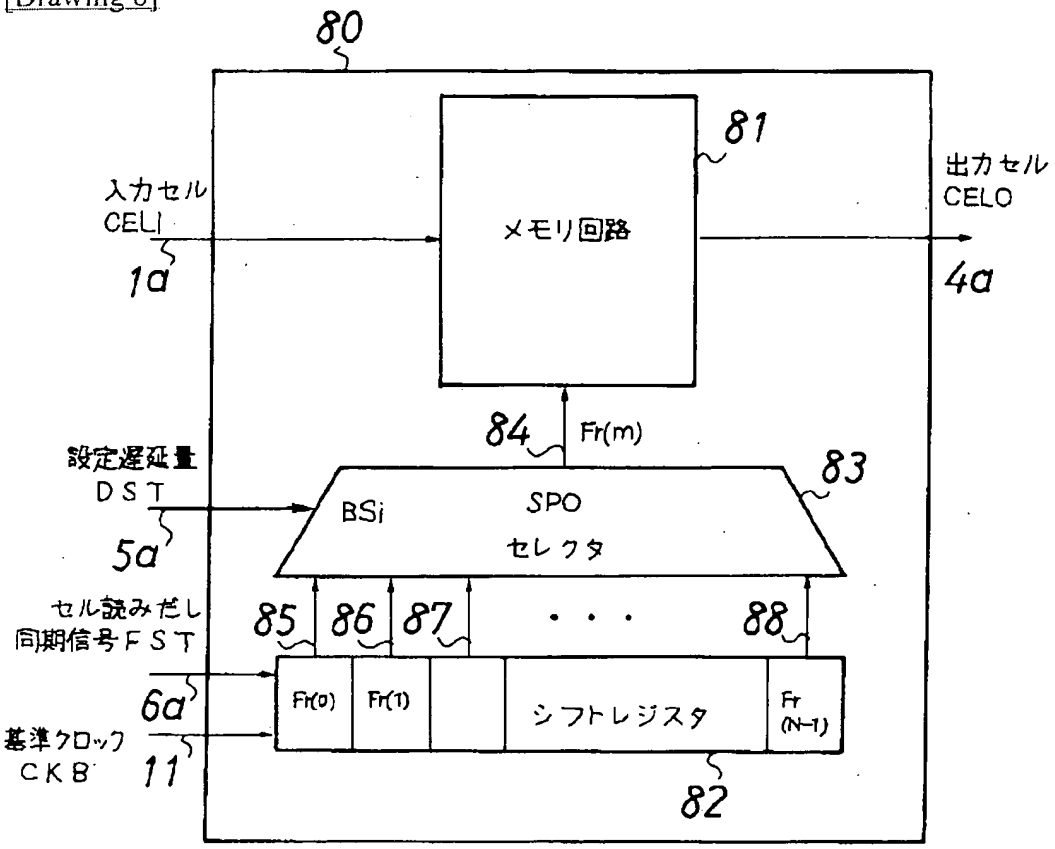
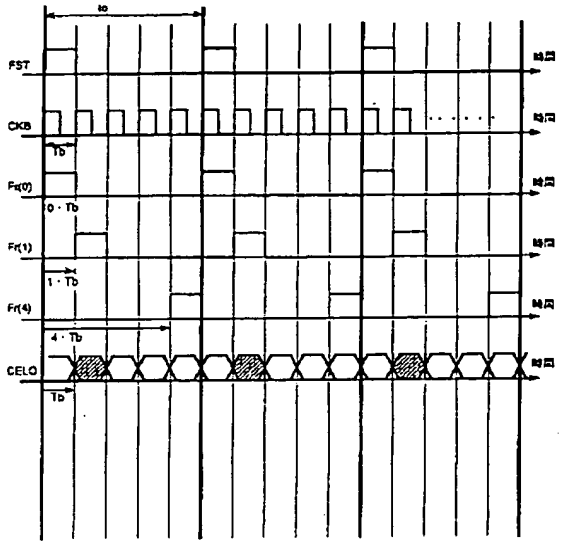
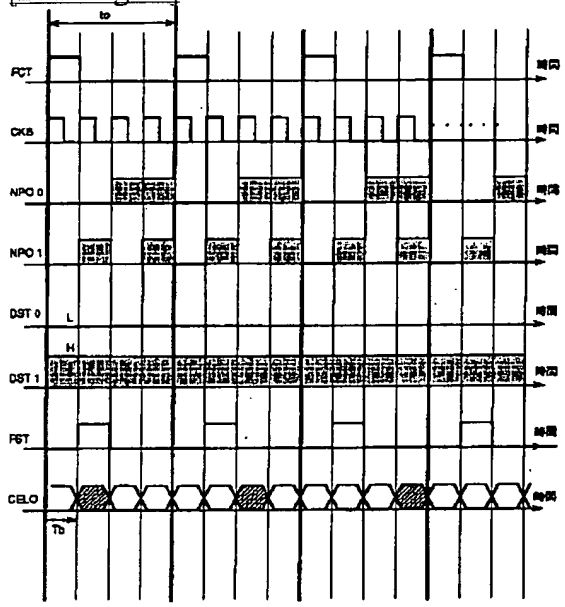


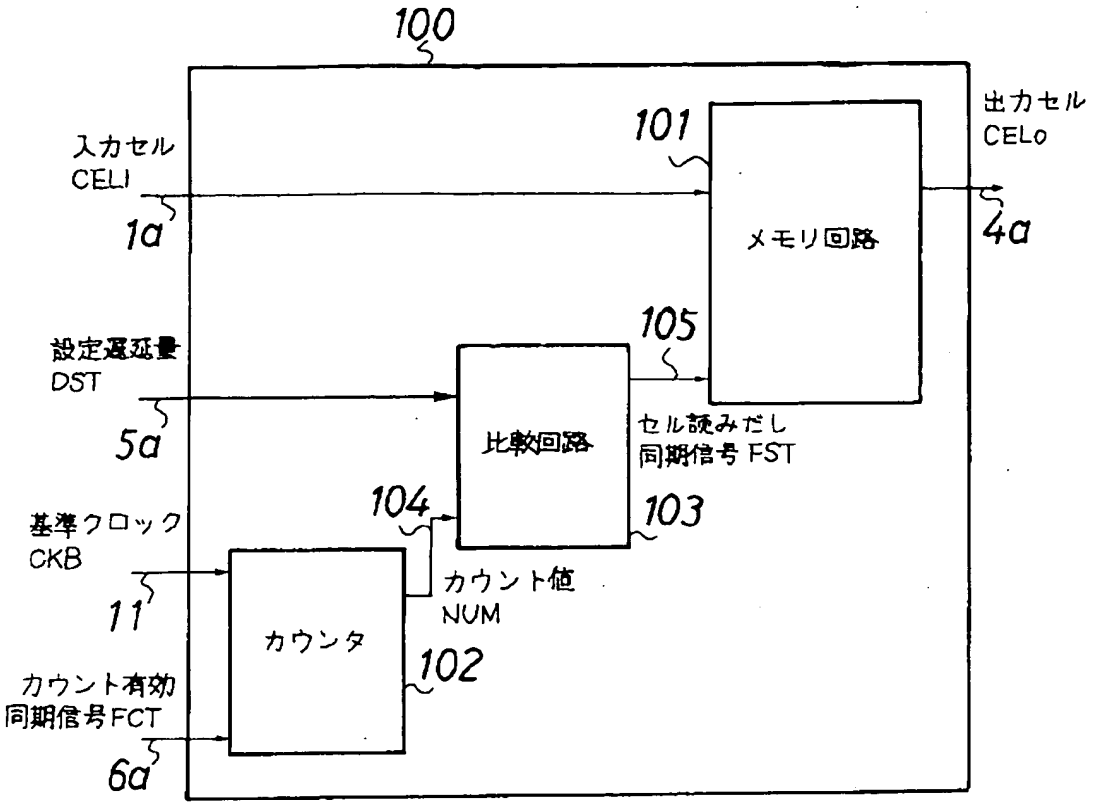
[Drawing 9]



[Drawing 11]



[Drawing 10]



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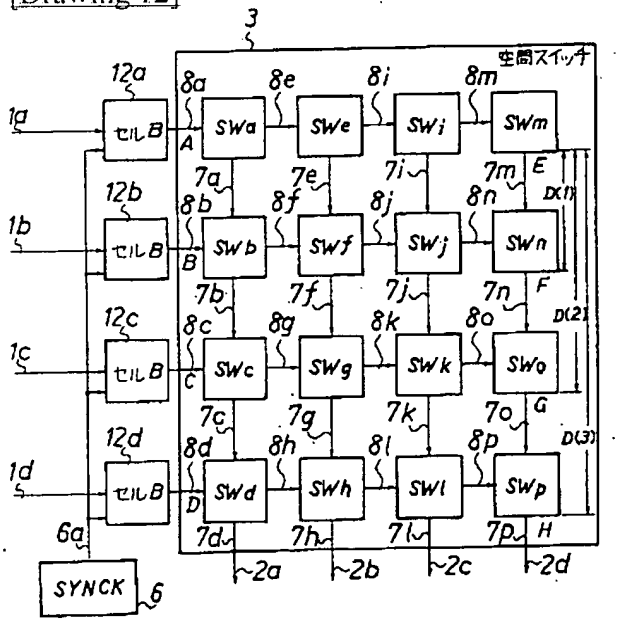
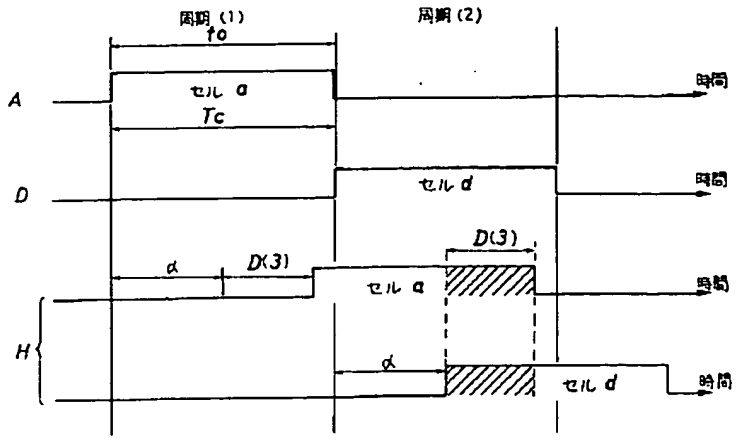


[Drawing 13]



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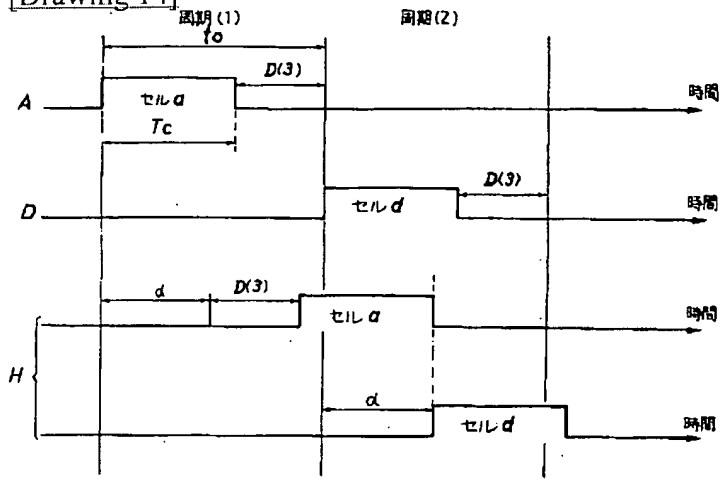

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First Hit

End of Result Set

L6: Entry 1 of 1 File: DWPI Jun 14, 2001

DERWENT-ACC-NO: 2001-380574
DERWENT-WEEK: 200145

TITLE: Multirate asynchronous transfer mode switching system has cell demultiplexer to distribute flow of incoming ATM cells to input ports of ATM switch in ATM cell arrival order

INVENTOR: MATSUMURA, K

PATENT-ASSIGNEE: NEC CORP (NIDE)

PRIORITY-DATA: 1999JP-0350778 (December 9, 1999)

Search Selected | Search ALL | Clear

PATENT-FAMILY:

	PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
☐	US 20010003528 A1	June 14, 2001		015	H04L012/56
☐	CA 2327930 A1	June 9, 2001	E	000	H04L012/56
☐	AU 200072150 A	June 14, 2001		000	H04L012/56
☐	JP 2001168866 A	June 22, 2001		013	H04L012/28
☐	EP 1107517 A2	June 13, 2001	E	000	H04L012/56

DESIGNATED-STATES: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
US20010003528A1	December 8, 2000	2000US-0731697	
CA 2327930A1	December 8, 2000	2000CA-2327930	
AU 200072150A	December 11, 2000	2000AU-0072150	
JP2001168866A	December 9, 1999	1999JP-0350778	
EP 1107517A2	December 8, 2000	2000EP-0126961	

INT-CL (IPC): H04 L 12/28; H04 L 12/56; H04 Q 11/04

ABSTRACTED-PUB-NO: US20010003528A
BASIC-ABSTRACT:

NOVELTY - Cell demultiplexer (25) distributes flow of incoming asynchronous transfer mode (ATM) cells to predetermined input ports of the ATM switch (26) in the ATM cell arrival order. ATM switch transfers the ATM cells received at the

input ports to appropriate output ports in units of predetermined time period based on the header information of each ATM cell. Cell multiplexer (27) multiplexes the outgoing ATM cells received in parallel from the output ports of the ATM switch to produce a flow of outgoing ATM cells.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for multirate switching method.

USE - Multirate asynchronous transfer mode (ATM) switching system.

ADVANTAGE - Simplifies cell flow control in an ATM switching system and simplifies cell demultiplexing control and cell multiplexing control at the input and output stages and thereby reduces the amount of hardware required.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the outline of configuration of multirate ATM switching system.

Cell demultiplexer 25

ATM switch 26

Cell multiplexer 27

ABSTRACTED-PUB-NO: US20010003528A
EQUIVALENT-ABSTRACTS:

CHOSEN-DRAWING: Dwg.1/7

DERWENT-CLASS: W01
EPI-CODES: W01-A03; W01-A03B1; W01-A06E1; W01-A06G2;